UNITED STATES PATENT APPLICATION FOR:

HOMOGENEOUS COPPER-PALLADIUM ALLOY PLATING FOR ENHANCEMENT OF ELECTRO-MIGRATION RESISTANCE IN INTERCONNECTS

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HOMOGENEOUS COPPER-PALLADIUM ALLOY PLATING FOR ENHANCEMENT OF ELECTRO-MIGRATION RESISTANCE IN INTERCONNECTS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims benefit of United States provisional patent application serial number 60/415,593, filed October 2, 2002, which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] Embodiments of the invention generally relate to a method and apparatus for depositing a layer of a metal or metal alloy into a high aspect ratio feature on a semiconductor substrate.

Description of the Related Art

[0003] Metallization of sub-quarter micron sized features is a foundational technology for present and future generations of integrated circuit manufacturing processes. More particularly, in devices such as ultra large scale integration-type (ULSI) devices, *i.e.*, devices having integrated circuits with more than a million logic gates, the multilevel interconnects that lie at the heart of these devices are generally formed by filling high aspect ratio interconnect features with a conductive material, such as copper or aluminum, for example. Conventionally, deposition techniques such as chemical vapor deposition (CVD) and physical vapor deposition (PVD), for example, have been used to fill these interconnect features. However, as interconnect sizes decrease and aspect ratios increase, void-free interconnect feature fill via conventional metallization techniques becomes increasingly difficult. As a result, plating techniques, such as electrochemical plating (ECP) and electroless plating, have emerged as viable processes for void free filling of sub-

quarter micron sized high aspect ratio interconnect features in integrated circuit manufacturing processes.

[0004] In an ECP process, for example, sub-quarter micron sized high aspect ratio features formed into the surface of a substrate may be efficiently filled with a conductive material, such as copper. ECP plating processes are generally two stage processes, in which a seed layer is first formed over the surface features of the substrate, and then the surface features of the substrate are exposed to an electrolyte solution, while an electrical bias is simultaneously applied between the substrate and an anode positioned within the electrolyte solution. The electrolyte solution is generally rich in ions to be plated onto the surface of the substrate, and therefore, the application of the electrical bias causes these ions to be plated onto the seed layer.

[0005] However, one challenge associated with ECP copper deposition processes is that the extremely small size of the conductive interconnect lines results in a substantial increase in the potential to form voids in the interconnect lines via electromigration modes. Inasmuch as the substantial increase in the potential to form voids in the interconnect lines via electromigration modes is directly related to the intrinsic electromigration (and/or stress migration) resistance of the copper line, it is desirable to generate conductive lines having minimal electrical resistance, while also having desirable electromigration characteristics. One method for improving the electromigration (and/or stress migration) resistance of copper lines is to alloy copper with a heavy metal without appreciably increasing the electrical resistance of the alloy when compared to copper, while simultaneously increasing the electromigration resistance characteristics of the alloy.

[0006] Palladium has been found to be a suitable alloying element that improves the electromigration (and/or stress migration) characteristic of copper plated layers.

However, current deposition techniques generally deposit individual layers of copper and palladium on top of each other, and then anneal the entire structure to form a copper-palladium alloy. This approach may be problematic, since the annealing process has been shown to form copper-palladium alloys having varying uniformity/homogeneity in cross-section that generates inconsistent conductive characteristics along the conductive lines, which may result in void formation. Additionally, although deposition of copper-palladium alloys via electrochemical deposition has been conventionally used to generate solder bump points and other larger scale features, conventional apparatuses and methods have not been successful in depositing a homogenous copper-palladium alloy into a high aspect ratio feature, *i.e.*, a feature where the height to width ratio is at least 4:1, without encountering voids in the fill deposition. Additionally, conventional copper-palladium alloy plating methods have focused upon alloys having large percentages of palladium and small concentrations of copper, which is undesirable for semiconductor device interconnects, since the electrical resistance characteristics of palladium rich alloys are substantially higher than copper or copper rich alloys. Void free fill of high aspect ratio features, such as those that make up the multilevel conductive interconnects in semiconductor devices, is critical to the continued success and continued progress of ULSI technology.

[0007] Therefore, a need exists for a method and apparatus for depositing a substantially homogenous copper-palladium alloy thin film into a high aspect ratio feature of a semiconductor device.

SUMMARY OF THE INVENTION

[0008] Embodiments of the invention are generally directed to a method for plating a homogenous copper-palladium alloy. The method includes providing a plating solution to an electrochemical plating cell. The plating solution includes a copper ion source at a concentration of between about 0.1 M and about 1.0 M and

a palladium ion source at a concentration of between about 0.0005 M and about 0.1 M. The method further includes supplying an electrical deposition bias to a plating surface. The electrical deposition bias is configured to simultaneously deposit copper ions and palladium ions onto the plating surface.

[0009] Embodiments of the invention are further directed to a method for electrochemically plating an alloy onto a semiconductor substrate. The method includes providing a plating solution containing copper ions and palladium ions, immersing a working surface of a substrate and an anode in the plating solution, and applying an electrical plating bias between the anode and the working surface. The electrical plating bias is configured to simultaneously plate copper and palladium out of the plating solution and onto the working surface.

[0010] Embodiments of the invention are further directed to a plating solution for plating a copper palladium alloy. The plating solution includes a source of copper ions, a source of palladium ions, an acid at a concentration of between about 5g/L about 200 g/L, and at least one plating solution additive configured to control plating characteristics.

[0011] Embodiments of the invention are further directed to an electrochemical plating cell configured to plate a homogenous copper-palladium alloy into features of a semiconductor device. The plating cell includes a substrate support member having a substantially planar lower surface configured to engage a non-production side of a substrate, an annular insulative cathode contact ring having a plurality of conductive substrate biasing members formed therein. Each of the plurality of conductive biasing members is configured to electrically engage a plating surface of a substrate. The plating cell further includes a plating cell container configured to hold a volume of electrochemical plating solution comprising a concentration of copper ions of between about 0.1 M and about 1.0 M and a concentration of palladium ions between about 0.0005 M and about 0.1 M, a power supply in

electrical communication with the plurality of conductive members and being configured to apply a plating bias to the plating surface, an anode positioned in the plating cell container in a position where the anode is immersed in the electrochemical plating solution, and a process controller programmed to ensure that the copper ion concentration in the plating solution is between about 0.1 M and about 1.0 M and the palladium ion concentration in the plating solution is between about 0.0005 M and about 0.1 M.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] So that the manner in which the above recited features of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0013] Figure 1 illustrates an exemplary weir-type plating cell of the invention.

[0014] Figure 2 illustrates an exemplary face down type plating cell of the invention.

[0015] Figure 3 illustrates a partial sectional perspective view of an exemplary electrochemical plating cell of the invention.

[0016] Figure 4 illustrates a current versus voltage schematic plot for individual deposition of copper and palladium.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Figure 1 illustrates a cross sectional view of an exemplary weir-type plater 100 of the invention. Plater 100 generally includes an electrolyte container 112 having an open top portion and a substrate holder 114 that is pivotally disposed above the electrolyte container 112, which contains an electrolyte solution. The substrate holder 114 is configured for immersing a substrate into the electrolyte solution and removing the substrate from the electrolyte solution. The substrate holder 114 is capable of securing and positioning the substrate in a desired position during processing.

[0018] A contact ring 120 is positioned proximate the lower surface of the lid/substrate holder 114, and is in electrical communication with a power supply (not shown). As such, the contact ring 120 is configured to electrically engage the substrate 122 and provide a plating bias to the substrate 122. The contact ring 120, which may be annular in shape, generally includes a plurality of conductive contact pins 126 distributed about a peripheral portion of the contact ring 120. The plurality of contact pins 126 generally extend radially below the perimeter of the substrate 122 such that the tips of the contact pins 126 contact a conductive seed layer formed on the substrate 122. Additionally, the electrolyte container 112 may include a separation membrane 128 positioned between an anode 116 and the substrate 122. The membrane 128 may operate to define respective anodic and cathodic chambers in the electrolyte container 112, *i.e.*, the anodic chamber will surround the anode and the cathodic chamber will be adjacent the plating surface of the substrate. The anode 116 is configured to supply ions to a plating solution contained within container 112. The separation membrane 128 is generally a membrane configured to allow the plating solution supplied to the container 112 to flow therethrough, while restricting the flow of other materials, *i.e.*, contaminants, copper balls, etc., from flowing through the membrane 128 and contacting the substrate 122. The plating solution is supplied to the electrolyte container 112 by a

supply line 118, which is generally in fluid communication with a pump and an electrolyte supply system, as is known in the art.

[0019] Additionally, the separation membrane 128 may also be configured to prevent the Pd^{2+} ions from penetrating into the anode chamber. The anodic chamber may also be configured to have a positive pressure with respect to the cathodic chamber so that a fluid flow exists only in the direction towards the cathodic chamber.

[0020] A process controller 190 is connected to the plater 100 for instructing the plater 100 to perform one or more processing steps associated with embodiments of the invention. The process controller 190 may include a CPU, which may be any form of computer processors that can be used in an industrial setting for controlling various chambers and subprocessors, and a memory for storing information and instructions to be executed by the CPU.

[0021] Figure 2 illustrates a cross sectional view of another exemplary electroplating process cell 200 of the invention. Process cell 200 generally includes a head assembly 210, a process kit 220, and an electrolyte collector 240. The electrolyte collector 240 is generally configured to be secured onto a mainframe (not shown) of a plating system (not shown). The electrolyte collector 240 generally includes an inner wall 246, an outer wall 248, and a bottom 247 connecting the respective walls. An electrolyte outlet 249 is disposed through the bottom 247 of the electrolyte collector 240 and connected to an electrolyte replenishing system (not shown) through tubes, hoses, pipes or other fluid transfer connectors. The head assembly 210 is generally mounted onto a head assembly frame 252 that includes a mounting post 254 and a cantilever arm 256. The mounting post 254 is generally mounted onto a mainframe body 214, and the cantilever arm 256 generally extends laterally from an upper portion of the mounting post 254. Generally, the mounting post 254 provides rotational movement with respect to a

vertical axis along the mounting post 254 to allow rotation of the head assembly 210. The lower end of the cantilever arm 256 is generally connected to a cantilever arm actuator 257, such as a pneumatic cylinder, mounted on the mounting post 254. The cantilever arm actuator 257 provides pivotal movement of the cantilever arm 256 with respect to the joint between the cantilever arm 256 and the mounting post 254.

[0022] The head assembly 210 generally includes a substrate holder assembly 250 and a substrate assembly actuator 258. The substrate assembly actuator 258 operates to rotate and/or raise/lower the substrate holder assembly 250. The substrate holder assembly 250 generally includes a substrate holder 264 and an integrally formed cathode contact ring 266. The substrate holder assembly 250 includes a plurality of vacuum channels 267 formed in a lower side of the substrate holder assembly 250. The vacuum channels 267, which are generally in communication with a vacuum pump (not shown), are annularly positioned about the lower surface of the substrate holder assembly 250 and configured to provide sufficient vacuum pressure to secure a substrate thereto for processing. The contact ring 266, which is generally in electrical communication with a power supply (not shown), includes an annular body having a plurality of conducting members disposed thereon for communicating electrical energy from the power supply to a substrate positioned on the holder assembly 250. The annular body of the contact ring 266 is generally constructed of an insulating material in order to electrically isolate the plurality of conducting members from surrounding components other than the substrate. The body and conducting members of the contact ring 266 generally form a diametrically interior substrate-seating surface which, during processing, may support the substrate being processed by process cell 200. The contact ring 266 is configured to electrically engage and contact the substrate being processed on the non-production side of the substrate, *i.e.*, on the backside of the substrate, so that the production side of the substrate is free of electrical or mechanical contacts therewith. As such, substrates processed in process cell 200

will generally have a backside conductive layer configured to electrically engage the backside contact ring deposited thereon. Additionally, the backside conductive layer, which is generally a seed layer extension, may be configured to communicate electrical power applied thereto to the front or production side of the substrate in order to cause plating thereon.

[0023] A process controller 290 is connected to the process cell 200 for instructing the process cell 200 to perform one or more processing steps associated with embodiments of the invention. The process controller 290 may include a CPU, which may be any form of computer processors that can be used in an industrial setting for controlling various chambers and subprocessors, and a memory for storing information and instructions to be executed by the CPU.

[0024] Figure 3 illustrates a perspective and partial sectional view of another exemplary electrochemical plating cell 300 of the invention. Plating cell 300 generally includes an outer basin 301 and an inner basin 302 positioned within outer basin 301. Inner basin 302 is generally configured to contain a plating solution that is used to plate a metal, e.g., copper, onto a substrate during an electrochemical plating process. During the plating process, the plating solution is generally continuously supplied to inner basin 302 (at about 1 gallon per minute for a 10-liter plating cell, for example), and therefore, the plating solution continually overflows the uppermost point of inner basin 302 and runs into outer basin 301. The overflow plating solution is then collected by outer basin 301 and drained therefrom for recirculation into basin 302. As illustrated in Figure 3, plating cell 300 is generally positioned at a tilt angle, *i.e.*, the frame portion 303 of plating cell 300 is generally elevated on one side such that the components of plating cell 300 are tilted between about 3° and about 30°. Therefore, in order to contain an adequate depth of plating solution within inner basin 302 during plating operations, the uppermost portion of basin 302 may be extended upward on one side of plating cell 300, such that the uppermost point of inner basin 302 is generally horizontal and

allows for contiguous overflow of the plating solution supplied thereto around the perimeter of basin 302.

[0025] The frame member 303 of plating cell 300 generally includes an annular base member 304 secured to frame member 303. Since frame member 303 is elevated on one side, the upper surface of base member 304 is generally tilted from the horizontal at an angle that corresponds to the angle of frame member 303 relative to a horizontal position. Base member 304 includes an annular or disk shaped recess formed therein, the annular recess being configured to receive a disk shaped anode member 305. Base member 304 further includes a plurality of fluid inlets/drains 309 positioned on a lower surface thereof. Each of the fluid inlets/drains 309 are generally configured to individually supply or drain a fluid to or from either the anode compartment or the cathode compartment of plating cell 300. Anode member 305 generally includes a plurality of slots 307 formed therethrough, wherein the slots 307 are generally positioned in parallel orientation with each other across the surface of the anode 305. The parallel orientation allows for dense fluids generated at the anode surface to flow downwardly across the anode surface and into one of the slots 307. Plating cell 300 further includes a membrane support assembly 306. Membrane support assembly 306 is generally secured at an outer periphery thereof to base member 304, and includes an interior region 308 configured to allow fluids to pass therethrough via a sequence of oppositely positioned slots and bores. The membrane support assembly may include an o-ring type seal positioned near a perimeter of the membrane, wherein the seal is configured to prevent fluids from traveling from one side of the membrane secured on the membrane support 306 to the other side of the membrane.

[0026] A process controller 390 is connected to the process cell 300 for instructing the process cell 300 to perform one or more processing steps associated with embodiments of the invention. The process controller 390 may include a CPU, which may be any form of computer processors that can be used in

an industrial setting for controlling various chambers and subprocessors, and a memory for storing information and instructions to be executed by the CPU.

[0027] In operation, regardless of the plating cell configuration utilized, a substrate to be plated is generally secured to a substrate support member and the plating surface of the substrate is brought into contact with a plating solution. While in contact with the plating solution, an electrical bias is applied to a seed layer deposited on the plating surface of the substrate. The electrical bias is generally a bias configured to bias the substrate surface/seed layer with a cathodic charge, which causes the plating ions in the plating solution to be urged out of the solution and to plate on the cathodically charged substrate surface/seed layer.

[0028] In conventional plating systems, the plating solution generally includes an aqueous solution that contains sulfuric acid, phosphoric acid, or derivatives thereof. The electroplating solution may further include one or more organic additives, *i.e.*, levelers, suppressors, accelerators, and/or other additives known in the art to facilitate control over the plating process. The additives are typically organic materials that are known to adsorb onto the surface of the substrate being plated. Useful suppressors, for example, may include polyethers, such as polyethylene, glycol, or other polymers such as polypropylene oxide, that are known to inhibit the rate of deposition on the substrate. Useful accelerators, for example, may include sulfides or disulfides, such as bis (3-sulfopropyl) disulfide, which affects the microstructure of copper deposited on the substrate. Useful levelers may generally include amines or polyamines, which improve the thickness distribution of copper deposited on the substrate.

[0029] Inasmuch as the present invention is configured to deposit a homogenous copper-palladium alloy in an electrochemical plating process, conventional copper plating solutions may be modified to include the palladium ions necessary to support copper-palladium plating. However, the amount of copper

and palladium deposited in an electrochemical plating process is generally governed by two factors: first, the plating potential at which plating operations are conducted; and second, the concentration of palladium ions in the plating solution in proportion to the concentration of the copper ions in the solution. As a result of the resistivity of copper being limited by the concentration of palladium ions, the amount of palladium in the plated alloy may be limited to less than about 2 weight percent, preferably, between about 0.2 weight percent and about 1.5 weight percent. In one embodiment, it is desirable to maintain the palladium percentage in the plated alloy below about 1.5 weight percent to provide good conductivity characteristics as well as good electromigration characteristics when compared to conventional copper interconnects. In another embodiment, the plated alloy has about 1.5 weight percent of palladium versus about 98.5 weight percent or more of copper. Additionally, any local agglomeration of palladium, which results from high concentrations of palladium in the plating solution or the copper-palladium alloy generated, will also produce disadvantages. Therefore, embodiments of the invention contemplate calculated concentrations of palladium configured to generate optimal plating characteristics without forming intermetallics, wherein the calculated concentrations of palladium are generally substantially smaller than the concentrations of the copper in the plating solution.

[0030] With regard to the plating potential used in plating a homogenous copper-palladium thin film, it is known that specific plating potential ranges result in optimized plating of specific metals. Therefore, in order for a copper-palladium alloy to be plated from a unitary plating solution, the plating potential applied during plating operations will generally overlap the plating potential ranges for both metals. As such, when the plating potential applied is resident in the plating ranges for both metals, simultaneous plating of both metals may be conducted. It is to be noted, however, that the plating potential for metals varies with the concentration of the metal ions in the plating solution, along with other parameters. As such, particular processing parameters will vary from processing system to processing system.

However, for reference, the standard reduction potential for copper is 0.34 volts with respect to a standard hydrogen electrode, while the standard reduction potential for palladium is 0.95 volts with respect to a standard hydrogen electrode. The change in the reduction potential resulting from concentration variances may generally be calculated by the following equation:

$$E = E_0 - R \cdot T \cdot \ln[M^+], \qquad (1)$$

wherein E generally represents the deposition potential of the metal, E_0 represents the standard deposition potential, R represents a constant, T represents the temperature of the plating solution (which is generally at room temperature (15 °C - 25°C)), and M^+ represents the concentration of the metal ions being plated in the plating solution. Therefore, since the standard deposition/reduction potential of palladium is substantially greater than the standard deposition potential of copper, the reduction potential of palladium may be brought closer to the reduction potential of copper via manipulation of the processing parameters noted in equation (1). However, although equation (1) indicates that the reduction potentials for copper and palladium may be brought closer in order to facilitate homogenous plating of a copper-palladium alloy, changes in ion concentrations alone generally do not result in large changes in the reduction potential of a metal. Additionally, conventional copper plating systems are generally optimized to achieve void free fill of high aspect ratio features, and therefore, it is not desirable to modify the copper ion concentration in the plating solution in order to achieve simultaneous copper and palladium plating, as the copper plating characteristics may suffer from this modification. As such, another parameter that is adjusted in order to obtain efficient and simultaneous plating of both copper and palladium is the plating potential or current density applied to the substrate surface during the plating process.

[0031] Figure 4 illustrates a current versus voltage schematic plot 400 for deposition of copper and palladium individually. The standard reduction potential

for copper is 0.34 volts with respect to a standard hydrogen electrode, while the standard reduction potential for palladium is 0.95 volts with respect to a standard hydrogen electrode. In one embodiment, the measurements are taken at room temperature, which is about 20 degrees Centigrade. At a cathodic potential of V_1, the amount of palladium deposition is represented by Pd_1 and the amount of copper deposition is represented by Cu_1. At a cathodic potential of V_2, the amount of palladium deposition is represented by Pd_2 and the amount of copper deposition is represented by Cu_2. As the cathodic potential is increased from V_1 to V_2, the amount of copper deposition increases from Cu_1 to Cu_2, while the amount of palladium deposition remains generally about the same, thereby decreasing the amount of palladium concentration in the alloy. The concentration of Pd^{2+} ions in the electrolyte is small enough such that the reduction of Pd^{2+} to Pd is mass-transfer controlled. The same effect, to a limited extent, may be accomplished by decreasing the concentration of palladium ions (Pd^{2+}) in the plating solution, while keeping the Cu^{2+} concentration constant. By decreasing the concentration of palladium ions in the plating solution, the amount of palladium in the alloy is also decreased. Alternatively, although generally undesirable in conventional plating systems for the reasons noted above, the same effect maybe accomplished by increasing the concentration of the copper ions (Cu^{2+}) in the plating solution. Therefore, in view of the parameters that may be modified in order to facilitate simultaneous copper-palladium deposition, embodiments of the invention contemplate that the following processing parameters will allow for the formation of a substantially homogenous copper-palladium alloy thin film in an electrochemical plating cell.

[0032] In accordance with an embodiment of the invention, a copper plating solution may be used to implement the formation of a substantially homogenous copper-palladium alloy thin film in an electrochemical plating cell. A conventional copper plating solution may include, for example, a copper source, a halide source, and one or more organic additives configured to provide a control element over the

plating characteristics of the plating solution. Copper plating solutions are commercially available from companies such as Enthone and Shipley, for example. The copper source for electrochemical plating solutions may be a copper sulfate solution having a copper ion concentration of between about 5 g/L and about 100 g/L. The plating solution may additionally contain an acid, which may be at a concentration of between about 5 g/L and about 200 g/L. The plating solution may further contain halide ions, such as chloride, which may be at a concentration of between about 10 ppm and about 200 ppm. Exemplary acids that may be used in plating solution include sulfuric acid, phosphoric acid, and/or derivatives thereof. In addition to using copper sulfate as the copper source, embodiments of the invention contemplate that the plating solution may include other copper salts, such as copper fluoborate, copper gluconate, copper sulfamate, copper sulfonate, copper pyrophosphate, copper chloride, or copper cyanide, for example, as the copper source. Embodiments of the invention, however, are not limited to these parameters.

[0033] The plating solution additives, which may include levelers, inhibitors, suppressors, brighteners, accelerators, and/or other additives known in the art, are typically organic materials that adsorb onto the surface of the substrate being plated. Useful suppressors typically include copolymers–ethylene oxide, propylene oxide, polyethers, such as polyethylene glycol (PEG), and/or other polymers, such as polyethylene-polypropylene oxides, which adsorb on the substrate surface, slowing down copper deposition in the adsorbed areas. Useful accelerators typically include sulfides or disulfides, such as bis (3-sulfopropyl) disulfide, MPSA, and SPS molecules, which compete with suppressors for adsorption sites, accelerating copper deposition in adsorbed areas. Useful levelers typically include amines, thiadiazole, imidazole, and other nitrogen containing organics. Useful inhibitors typically include sodium benzoate and sodium sulfite, which inhibit the rate of copper deposition on the substrate.

[0034] During plating, the additives are generally consumed at the substrate surface. As such, plating systems generally include a replenishment mechanism configured to replace the additives consumed in the plating process so that a relatively constant concentration of the additives may be maintained in the plating solution. However, it is generally known that differences in diffusion rates of the various additives may result in varying concentrations of particular additives at the top of a high aspect ratio feature compared to the bottom of the feature, thereby setting up different plating rates at the top of the feature versus the bottom of the feature. For example, suppressors may be larger molecules that diffuse slower than accelerators, and therefore, fewer suppressors may adsorb onto the bottom surface of a high aspect ratio feature than accelerators. As such, the bottom of the feature may plate at a faster rate than the top of the feature, thus increasing the fill rate of the feature. Therefore, an appropriate composition of additives in the plating solution is desired to facilitate void-free fill of high aspect ratio features.

[0035] In order to simultaneously plate both copper and palladium, embodiments of the invention contemplate adding a source of palladium ions to the above noted copper plating solution. The source for the palladium ions includes, for example, $PdSO_4$, $PdCl_2$, or other palladium containing compounds acceptable to a copper electrochemical plating solution. The concentration of the palladium ions in the plating solution is generally between about 0.0005 M and about 0.1 M, while the concentration of the copper ions in the plating solution is generally between about 0.1 M and about 1 M. In another embodiment of the invention, the copper concentration in the plating solution may be between about 0.4 M and about 0.8 M. The plating current density applied to the substrate during a copper-palladium electrodeposition process using the copper-palladium plating solution described above may be between about 0.5 mA/cm^2 and about 80 mA/cm^2, for example, at a constant current density. Alternatively, the plating current density may be varied throughout the copper-palladium deposition process, *i.e.*, the current density may be stepped up, down, or alternated between lower and higher current densities, *i.e.*,

pulsed, during a plating process. For example, the current density may be calculated to facilitate copper-palladium deposition in an initial stage of filling a feature, and then the current density may be changed to facilitate a more copper heavy deposition once the feature is somewhat lined with a copper-palladium alloy at the interfaces. Additionally, the substrate support member supporting the substrate during the copper-palladium electrodeposition process is generally rotated at between about 5 RPM and about 60 RPM, for example, while the flow rate of the copper-palladium electroplating solution to the electroplating cell is up to about 7.5 GPM, for example. Embodiments of the invention contemplate that the plating cell is capable of providing generally constant hydrodynamics so that the flow of the plating solution across the plating surface of the substrate is constant. In this manner, a fresh supply of both copper and palladium ions is maintained at the plating surface, which is important to simultaneous plating operations, since one ion may generally deplete faster than another ion and cause non-uniformity (spatial non-homogenous alloys) in the alloy layer.

[0036] Once the homogenous copper-palladium layer is deposited, the layer may be annealed. The annealing process may contribute to the grain size determination, the grain distribution in the alloy, and the crystalline structure of the alloy. Embodiments of the invention contemplate that an annealing process may be implemented to anneal the homogenous copper-palladium alloy films, wherein the annealing process includes exposing the film to a temperature of between about 200° C and about 400° C, for example. The exposure/annealing time for the copper-palladium film may be between about 30 seconds and about 1 hour, depending upon the structure desired and the thermal budget available for the process. The resulting substantially homogenous copper-palladium layer will generally have a palladium concentration of up to about 2 weight percent. More particularly, the homogenous copper-palladium alloy of the invention may have a palladium concentration of between about 0.2 weight percent and about 1.5 weight

percent, or between about 0.1 weight percent and about 0.6 weight percent, for example.

[0037] Accordingly, various embodiments of the invention generally provide a method and apparatus for forming a substantially homogenous copper-palladium alloy layer onto a semiconductor substrate, and in particular, for filling high aspect ratio (4:1 or higher) features with a substantially homogenous copper-palladium alloy that has a large concentration of copper (above about 98.5 weight percent) and a substantially smaller concentration of palladium (about 0.2 weight percent to about 1.5 weight percent). The copper-palladium alloy, which provides enhanced electromigration and/or stress migration resistance in conductive features of semiconductor devices and prevents the formation of voids at the interfaces when high current is passed through the interconnect, is generally formed onto the substrate and into the features via an ECP process. Embodiments of the ECP process for depositing the copper-palladium alloy generally include adding a calculated amount of palladium to a copper plating solution and applying a calculated voltage to a substrate immersed in the plating solution. The calculated amount of palladium added to the plating solution and the calculated voltage applied are specifically selected to provide for the deposition of a substantially homogenous copper-palladium alloy. Additionally, embodiments of the invention are configured to plate the copper-palladium alloy into very high aspect ratio features, e.g., greater than 10:1, for narrow conductive structures, *i.e.*, sub 0.10 micron width features. The deposition of the copper-palladium alloy may also be accomplished by depositing a very thin copper-palladium layer on a PVD copper seed layer by an electroless deposition process followed by electroplating the copper-palladium alloy in the plating solution described below.

[0038] Embodiments of the invention may be used in connection with a device for measuring component quantities for use in apparatus implementing multiple chemistries, as described in US patent application serial no. _____

(AMAT/8465/CMP/ECP/RKK), entitled VOLUME MEASUREMENT APPARATUS AND METHOD, by Balisky et al, filed October 1, 2003, which is incorporated herein by reference. The measurement device may be used for measuring, adding, or mixing chemical components for various plating processes, including direct plating on a barrier layer, alloy plating, alloy plating combined with convention metal plating, plating on a thin seed layer, optimized feature fill and bulk fill plating, plating multiple layers with minimal defects, or any other plating process where more than one chemistry may be beneficial to a plating process.

[0039] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.